**What is claimed is:**

1. A method of synchronizing an internal clock in a communications system comprising:
   a) extracting a timestamp from a received signal;
   b) determining a difference between the timestamp and a time value of the internal clock; and
   c) modifying a rate of change of the internal clock when the magnitude of the difference exceeds a rate of change threshold.
2. The method as in claim 1, preceded by extracting a first timestamp from the received signal and setting the time value of the internal clock to a value derived from the first timestamp.
3. The method as in claim 1, further including setting the time value to a value determined from the timestamp when the difference exceeds a timing threshold.
4. The method as in claim 1, wherein modifying the rate of change is preceded by:
   i) incrementing a fault counter if the difference exceeds a timing threshold;
   ii) setting the time value to a value determined from the timestamp, setting the difference to zero, and setting the fault counter to zero when the fault counter exceeds a fault threshold;
5. The method as in claim 1, wherein modifying the rate of change further includes replacing a set of N clock cycles, each comprising M pulses, with A clock cycles, each comprising B pulses, such that N×M is equal to A×B.
6. The method as in claim 5, wherein A > N.
7. The method as in claim 5, wherein A < N.
8. The method as in claim 1, wherein modifying the rate of change includes decreasing the rate of change when the time value leads the timestamp.
9. A method as in claim 1, wherein modifying the rate of change includes increasing the rate of change when the time value lags the timestamp.
10. A method of synchronizing an internal clock in a communications system comprising:
    a) extracting an original timestamp from a received signal;

b) setting a time value of the internal clock to a value derived from the original timestamp;

c) extracting a subsequent timestamp from the received signal;

d) determining the difference between the subsequent timestamp and the time value;

e) incrementing a fault counter if the magnitude of the difference exceeds a timing threshold;

f) resetting the clock to a value determined from the subsequent timestamp if the fault counter exceeds a fault threshold; and

g) modifying the rate of change of the internal clock if the difference exceeds a rate of change threshold and does not exceed a timing threshold.

11. A clock synchronization system comprising

a timestamp extractor, for extracting a timestamp from a data stream, and for deriving a time value from said timestamp; and

a clock controller, operatively attached to the timestamp extractor and an internal clock, said internal clock having a time value, for receiving select time values derived from a timestamp, and for digitally modifying the internal clock time value, in response to the timestamp derived time value.

12. The clock synchronization system, as in claim 11, wherein the clock controller includes a comparator, operatively connected to the timestamp extractor and the internal clock, for determining a difference between the timestamp derived time value and the internal clock time value.

13. The clock synchronization system, as in claim 11, wherein the clock controller includes an oscillator for controlling a rate of change of the internal clock.

14. The clock synchronization system, as in claim 13, wherein the clock controller includes means for increasing the rate of change when the internal clock lags the timestamp derived time value.

15. The clock synchronization system, as in claim 13, wherein the clock controller includes means for decreasing the rate of change when the internal clock leads the timestamp derived time value.

16. An internal clock synchronization system comprising:

a comparator, having first and second inputs for receiving first and second input signals, for determining a difference between the first and second input signals and providing at a comparator output a difference signal representative of the determined difference;

a clock controller, operatively connected to the comparator output, for receiving the difference signal and for digitally deriving a timing correction signal therefrom, and for providing the digitally derived timing correction signal at a clock controller output;

a timestamp extractor, operatively connected to the first input of the comparator, for extracting a timestamp associated with a data unit and for providing a signal indicative of a timestamp value to the first input of the comparator; and

a clock, operatively attached to the clock controller output for receing the timing correction signal and operatively attached to the second input of the comparator for providing a signal indicative of an internal time value.

17. A system as in claim 16, wherein the clock controller further includes

a pattern table, for storing clock cycle patterns representative of different clock speeds;

a processor, operatively attached to the pattern table, for receiving the difference signal from the comparator output, and for retrieving clock cycle patterns from the pattern table based on the received difference signal, and for providing at a processor output a signal representative of the clock cycle pattern;

an oscillator, for providing at an oscillator output an oscillating signal; and

a pattern generator, operatively connected to the oscillator output and the processor output, for generating a digitally derived timing correction signal for the clock controller output based upon the oscillating signal and the signal from the processor.

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